



Atty. Docket No. 002187 USA/C03/PDC/WF/DB
PATENT APPLICATION

PRELIMINARY AMENDMENT
U.S. Application No. 09/765,995

Page 11, please delete the fourth full paragraph, and replace it with the following new paragraph:

Movement controller 13 further controls a two-dimensional scanning stage 22 effective, during the Phase II examination, to position the wafer at any desired position with respect to the Phase II detector 9 (the CCD matrix). As described in detail below, the control of one of the axes of this stage serves also during the Phase I examination. Movement controller 13 further controls a rotation/level/focus stage 23, which rotates the wafer about its axis to align it angularly, to level it, and to keep it in focus during scanning. Stage 23 also moves the vacuum chuck 24 and its wafer towards or away from the Phase II sensor 9 to enable producing a plurality of images at different depths during the Phase II examination, as will be described more particularly below.

Page 18, please delete the third full paragraph, and replace it with the following new paragraph:

The output of Decision Table 66 is applied to a parameters buffer circuit 68 which records the parameters describing each defect, such as the exact coordinates and the type (to be explained later) and intensity of the pixels in the immediate vicinity of the defect in both the inspected and reference images. It receives as inputs the alarm flag trigger ("0" indicates no defect, and "1" indicates a defect), and all the parameters to be recorded. The latter are received from temporary memories associated with each of the eight channels. The parameters buffer 68 outputs a list of the defects accompanied by their parameters to the post processor 14.

Atty. Docket No. 002187 USA/C03/PDC/WF/DB
PATENT APPLICATION

PRELIMINARY AMENDMENT
U.S. Application No. 09/765,995

Page 25, please delete the third full paragraph, and replace it with the following new paragraph:

The Ratio Calculator 70e computes the ratio between the current pixel P(ij), and the average of the pixels in the surrounding area in the vertical and horizontal directions. It outputs the following signals: the ratio in the horizontal direction (Rh); the ratio in the vertical direction (Rv); and the ratio to the average of the four surrounding pixels (Rij).

Pages 35-36, please delete paragraph bridging pages 35-36, and replace it with the following new paragraph:

Multiplier 86 also receives the output from the Summation Calculator 84 via the Division Table 85. Thus, the Summation Calculator 84 computes the absolute sum of the two matrices On which the processing will be carried out. It includes, for each Pixel Normalizer 81, 82, an Absolute Value Circuit 84a, 84b, which computes the absolute values of each normalized pixel; and a Matrix Sum Circuit 84c, 84d, which sums the nine absolute values.

Page 36, please delete the second full paragraph, and replace it with the following new paragraph:

Multiplier 86 computes the result of the normalized difference for the point under test. The computation is carried out using the formula:

$$\text{SCORE} = (\Sigma |P_L - P_R|) * [1/(\Sigma |P_L| + |P_R|)]$$

where P_L , P_R are the normalized values of the pixels.

Atty. Docket No. 002187 USA/C03/PDC/WF/DB
PATENT APPLICATION

PRELIMINARY AMENDMENT
U.S. Application No. 09/765,995

Page 36-37, please delete the paragraph bridging pages 36-37, and replace it with the following new paragraph:

The construction and operation of the Defect Detector, as illustrated for example in Fig. 14, will be better understood by reference to Figs. 24 and 25. As described earlier, the function of Comparator 77 is to carry out a comparison between the inspected image in the vicinity of the current pixel, and the reference image in the vicinity of the corresponding pixel, and to output an Alarm signal, via buffer 68 (Fig. 12), to the Post Processor 14 indicating whether or not there is a suspected defect. As also indicated earlier, the comparison is made with respect to a variable threshold level, which is dependent on the Type of the current pixel in the reference and inspected images.

Page 38, please delete the first full paragraph, and replace it with the following new paragraph:

Comparator 77 further includes nine conversion tables 77i for the low threshold level, and nine conversion tables 77j for the higher threshold levels. These tables are loaded prior to the inspection session. The tables are selected from a set of tables according to the required sensitivity of the detection, as set by the user. Their function is to multiply each one of the energies around the pixel being examined by a constant which depends both on the type of the examined pixel in the reference image, and the type of the current pixel in the inspected image.

Atty. Docket No. 002187 USA/C03/PDC/WF/DB
PATENT APPLICATION

PRELIMINARY AMENDMENT
U.S. Application No. 09/765,995

Page 39, please delete the second full paragraph, and replace it with the following new paragraph:

The post-processor 14 (Fig. 12) thus receives the list of suspected defects, together with their relevant parameters, and makes decisions before passing them onto the Phase II examination system. These decisions include: (a) clustering; (b) choosing the points which will be passed to Phase II; and (c) the optimum route in Phase II. The latter functions are carried out by microprocessor programs.

Page 49, please delete the second full paragraph, and replace it with the following new paragraph:

The information detected by the image converter 309 is fed to a preamplifier 320 in the preprocessor 310, then to a digitizer 321, and then to a memory buffer 322 in the image processor 311. The image processor 311 further includes a digital signal processor which, under software control (block 324) from the main controller (8, Fig. 2), performs a comparison operation 327, and a classification operation 328. Since the comparison distance (d) is small for typical repetitive patterns, it is assumed that the CCD frame contains at least two comparable units. Therefore, it does not perform a matching operation or a registration operation, corresponding to operations 123 and 126 in Fig. 27. The output from the digital signal processor 323 is then returned to the main controller.